

CLAIMS

What is claimed is:

- 1 *Sub* 1. A method of communicating between functional blocks comprising:  
 2 *G* Originating a packet;  
 3 passing the packet;  
 4 decoding the packet; and  
 5 utilizing the packet.
- 1 2. The method of claim 1 wherein:  
 2 originating is performed by a master.
- 1 3. The method of claim 2 wherein:  
 2 passing is performed by a first target.
- 1 4. The method of claim 3 wherein:  
 2 decoding is performed by the first target.
- 1 5. The method of claim 3 wherein:  
 2 decoding is performed by a second target.
- 1 6. The method of claim 5 wherein:  
 2 passing is performed by the second target

1 7. The method of claim 5 wherein:  
 2 utilizing is performed by the second target  
 3 and  
 4 passing is performed by the second target

1 8. The method of claim 7 further comprising:  
 2 removing the packet.

1 9. The method of claim 8 wherein:  
 2 the first target comprising a ring interface and a control, the second target  
 3 comprising a ring interface and a control, the master comprising a ring interface and a  
 4 control, a ring connecting to the ring interface of the first target, the ring interface of the  
 5 second target, and the ring interface of the master in a daisy chain fashion, the ring  
 6 used for the passing and the originating.

1 10. The method of claim 9 wherein:  
 2 the master performing the removing after the passing brings the packet back to  
 3 the master.

1 11. The method of claim 1 further comprising:  
 2 requesting a ring, the ring used for the originating and the passing; and  
 3 granting the ring.

1 12. The method of claim 11 wherein:  
2 the originating is performed by a first master.

1 13. The method of claim 12 wherein:  
2 the requesting is performed by a second master

1 14. The method of claim 13 wherein:  
2 the granting is performed by the first master.

1 15. The method of claim 13 wherein:  
2 the granting is performed by an arbitrator

1 16. The method of claim 11 further comprising:  
2 arbitrating between a first master requesting the ring and a second master  
3 requesting the ring.

1 17. A communications network comprising:  
2 a first master having a ring interface and a control;  
3 a first target having a ring interface and a control;  
4 a first ring connection coupling the ring interface of the first master to the ring  
5 interface of the first target;  
6 a second target having a ring interface and a control, the first ring connection for  
7 passing packets; and

8 a second ring connection coupling the ring interface of the first target to the ring  
9 interface of the second target, the second ring connection for passing packets; and  
10 a third ring connection coupling the ring interface of the second target to the ring  
11 interface of the first master, the third ring connection for passing packets.

1 18. The communications network of claim 17 wherein:  
2 the master originates a set of packets which are passed via the first ring  
3 connection to the first target

1 19. The communications network of claim 18 wherein:  
2 the first target passes the set of packets via the second ring connection to the  
3 second target; and  
4 the second target passes the set of packets via the third ring connection to the  
5 first master.

1 20. The communications network of claim 19 wherein:  
2 the first target comprises a first configuration block on an integrated circuit; and  
3 the second target comprises a second configuration block on the integrated  
4 circuit.

1 21. A communications network comprising:  
2 a first master;  
3 a first target;

4 a second target;  
 5 and a ring, the ring coupled to the first master, the ring coupled to the first target,  
 6 and the ring coupled to the second target.

1 22. The communications network of claim 21 further comprising:  
 2 a second master, the ring coupled to the second master

1 23. The communications network of claim 22 further comprising:  
 2 an arbitrator, the arbitrator coupled to the first master, the arbitrator coupled to  
 3 the second master, the arbitrator controlling activity of the first master and the second  
 4 master.

1 24. The communications network of claim 22 further comprising:  
 2 a request line, the request line coupled to the first master, the request line  
 3 coupled to the second master;  
 4 and a grant line, the grant line coupled to the first master, the grant line coupled  
 5 to the second master.

1 25. The communications network of claim 24 further comprising:  
 2 the request line configured to pass signals in a first direction, the grant line  
 3 configured to pass signals in a second direction.

1 26. The communications network of claim 25 wherein:  
2 the first direction and the second direction dynamically alterable.

1 27. The communications network of claim 22 further comprising:  
2 a request line, the request line coupled to the first master, the request line  
3 coupled to the second master, the request line coupled to the first target, the request  
4 line coupled to the second target.

1 28. The communications network of claim 27 wherein:  
2 the request line configured such that signals flow in a logically opposite direction  
3 to signals on the ring

1 29. The communications network of claim 28 wherein:  
2 the ring comprising a grant line and a set of data lines, the grant line configured  
3 to indicate a master may use the ring, the data lines configured to transmit signals.

1 30. The communications network of claim 29 wherein:  
2 the ring further comprising a packet valid line, the packet valid line configured to  
3 indicate whether a valid packet is being transmitted on the ring.

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2 *al*

31. The communications network of claim 21 wherein:  
the ring comprising a set of data lines, the data lines configured to transmit  
signals.

32. The communications network of claim 31 wherein:  
the first master utilizing the ring to transmit signals to the first target, the first  
target utilizing the ring to transmit signals to the second target, the second target  
utilizing the ring to transmit signals to the first master.

33. The communications network of claim 31 wherein:  
the first master comprising a ring interface coupled to the ring and a control  
coupled to the ring interface, the control suitable for generating packets, the packets  
transmitted through the ring interface to become signals on the ring.

34. The communications network of claim 33 wherein:  
the first target comprising a ring interface and a decoder coupled to the ring  
interface, the decoder receiving the signals that represent a packet, the decoder  
determining if the packet is addressed to the first target.

1 35. The communications network of claim 34 wherein:  
 2 the second target comprising a ring interface and a decoder coupled to the ring  
 3 interface, the decoder receiving the signals that represent a packet, the decoder  
 4 determining if the packet is addressed to the second target.

1 36. The communications network of claim 35 wherein:  
 2 a packet comprised of a header and a set of data, the header including an X  
 3 indication of the logical size of the set of data.

1 37. The communications network of claim 35 wherein:  
 2 a packet comprised of a fixed number of units of data, the units of data encoding X  
 3 an address.

1 38. The communications network of claim 21 wherein:  
 2 the first master, the first target and the second target on an integrated circuit.

1 39. The communications network of claim 21 wherein:  
 2 the first master and the first target on a first integrated circuit, the second target  
 3 on a second integrated circuit.



1 40. The communications network of claim 21 wherein:  
2 the first master on a first integrated circuit, the first target on a second integrated  
3 circuit.

1 41. The communications network of claim 22 wherein:  
2 the second master comprising a buffer, the buffer utilized for storing incoming  
3 data when the second master originates a packet, the incoming data passed after the  
4 second master completes origination of the packet.

1 42. A system comprising:  
2 a processor;  
3 a processor bus coupled to the processor;  
4 a data chip coupled to the processor bus; and  
5 an address chip coupled to the processor bus and coupled to the data chip;  
6 the address chip including a configuration ring, the configuration ring having a  
7 master, a first target and a second target, the master coupled through a ring to the first  
8 target, the first target coupled through the ring to the second target, the second target  
9 coupled through the ring to the master.

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